MOTOROLA
Semiconductor Products Sector

Order Number: MPC107UMAD/D
Rev. 0, 2/2001

PowerPC™

Errata to
MPC107 PCI Bridge/Memory Controller User's Manual, rev. 0

This errata describes corrections to the *MPC107 PCI Bridge/Memory Controller User's Manual*, rev 0. For convenience, the section number and page number of the errata item in the user's manual are provided.

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2.1.2, 2-7 In Table 2–2, the state of the $\overline{\text{INT}}$ signal during reset should read as follows:

Table 2–2. Output Signal States During System Reset

Interface	Signal	State During System Reset
—	—	—
EPIC control	$\overline{\text{INT}}$	Driven (unknown until $\overline{\text{HRESET}}$ is negated), then negated.
—	—	—

3.1, 3–2 In Table 3–1, the PCI address range for the processor address range 8000_0000 through FDFF–FFFF should read as follows:

Table 3–1. Address Map B—Processor View in Host Mode

Processor Address Range				PCI Address Range	Definition
Hex		Decimal			
—	—	—	—	—	—
8000_0000	FDFF_FFFF	2G	4G - 32M - 1	8000_0000–FDFF_FFFF	PCI memory space[3]
—	—	—	—	—	—

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3.1, 3–7	Replace Figure 3–3 with the following:

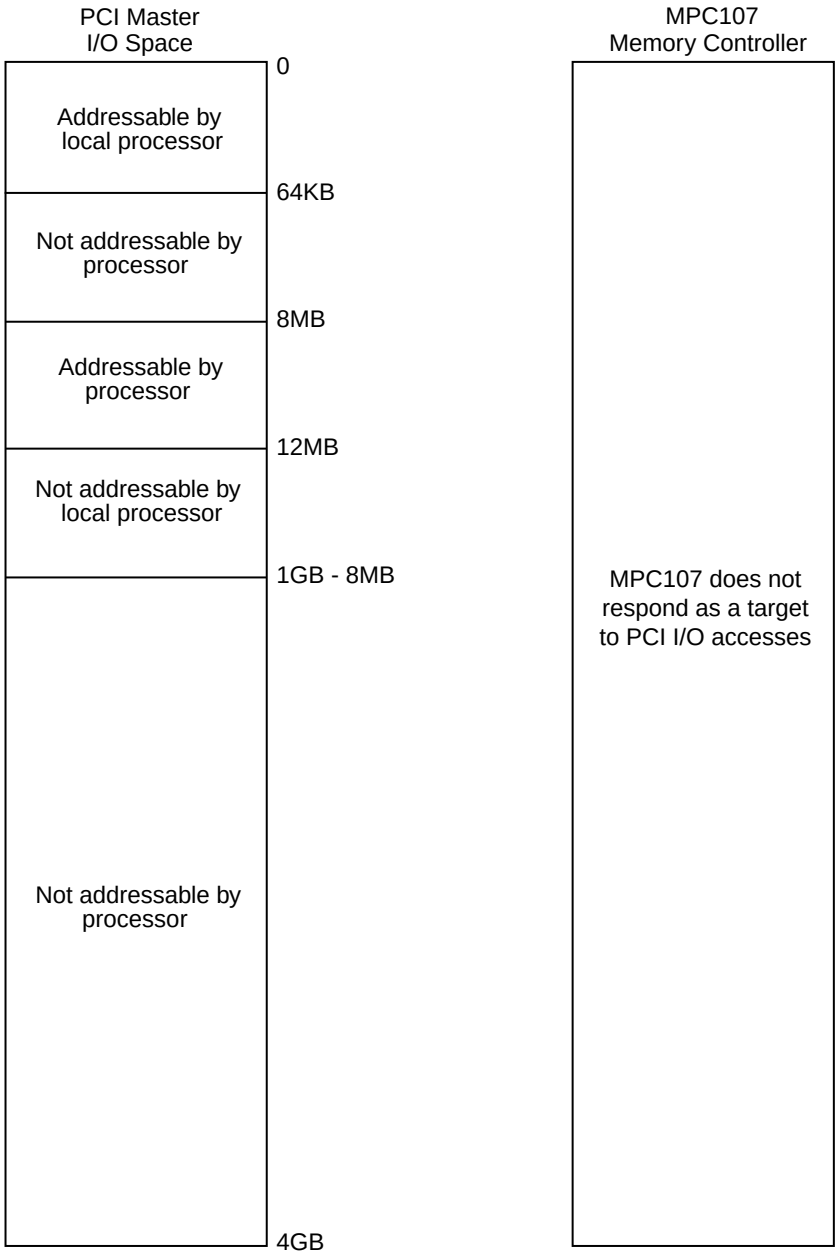

Figure 3-3. PCI I/O Master Address Map B

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4.1, 4–7 The reset value for the MCCR4 register should read as follows:

Table 4–2. MPC107 Configuration Registers Accessible from the Processor

Address Offset	Register	Size	Program Access Size (Bytes)	Access	Reset Value
—	—	—	—	—	—
0xFC	MCCR4	4 bytes	1, 2, or 4	Read/Write	0x0010_0000
—	—	—	—	—	—

4.7, 4–33 In Table 4–28, replace the name and description of the setting for bit 29 with the following:

Table 4–28. Bit Settings for PICR2—0xAC

Bits	Name	Reset Value	Description
29	SERIALIZE_ON_CFG	0	This bit controls whether the MPC107 serializes configuration writes to PCI devices from the processor. Note that the sense of this bit is the opposite of that on the MPC8240. 0 Configuration writes to PCI devices from the processor do not cause serialization. The internal buffers are not flushed. 1 Configuration writes to PCI devices from the processor cause the MPC107 to serialize and flush the internal buffers.

4.10, 4–47 Replace Figure 4–30 with the following. Note the name change to bit 18.

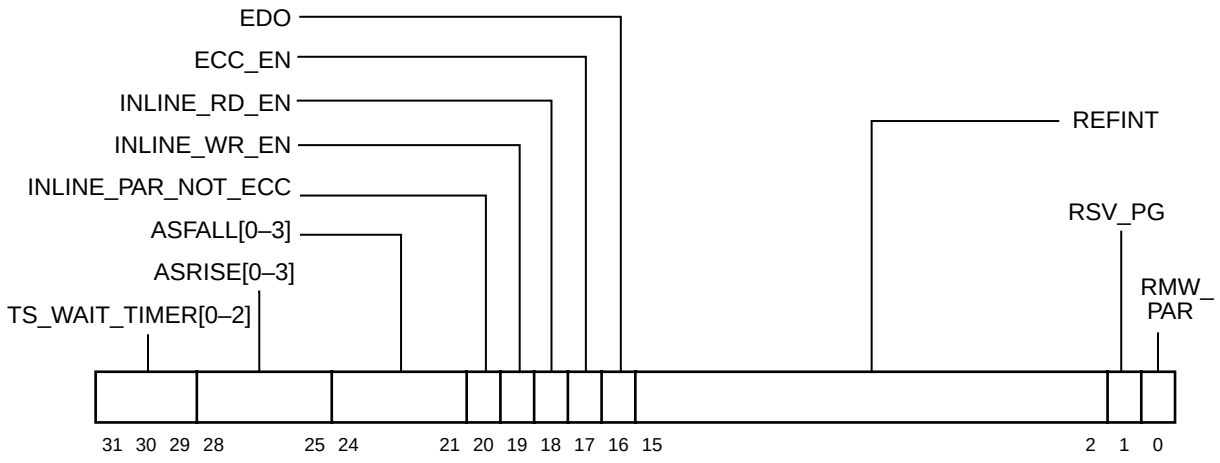

Figure 4–30. Memory Control Configuration Register 2 (MCCR2)—0xF4

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4.10, 4–48

In Table 4-40, replace the “Wait States for ROM High Impedance” table in the description for bits 31–29 with the following. Note the addition of rows for 011 and 110.

Table4–40. Bit Settings for MCCR2–0xF4

Bits	Name	Reset Value	Description
31–29	TS_WAIT_ TIMER[0–2]	000	Transaction start wait states timer. The minimum time allowed for ROM/Flash/Port X devices to enter high impedance is 2 memory system clocks. TS_WAIT_TIMER[0–2] adds wait states before the subsequent transaction starts in order to account for longer disable times of a ROM/Flash/Port X device. This delay is enforced after all ROM and Flash accesses, delaying the next memory access from starting (for example, DRAM after ROM access, SDRAM after Flash access, ROM after Flash access). Note that this parameter is supported for SDRAM systems only. For EDO/FPM DRAM systems, TS_WAIT_TIMER[0–2] must = 000.

Bits	Wait States for ROM High Impedance		
	Reads with wide data path (32 or 64-bit)	**Reads with gather data path in flow-through or registered buffer mode (8, 16, 32-bit)**	**All writes[1, 2] and reads with gather data path in in-line buffer mode (8, 16, 32,-bit)**
000	2 clocks	5 clocks	6 clocks
001	2 clocks	5 clocks	6 clocks
010	3 clocks	5 clocks	6 clocks
011	4 clocks	5 clocks	6 clocks
100	5 clocks	6 clocks	7 clocks
101	6 clocks	7 clocks	8 clocks
110	7 clocks	7 clocks	7 clocks
111	8 clocks	9 clocks	10 clocks

Note 1. In this context, Flash writes are defined as any write to $\overline{\text{RCS0}}$ or $\overline{\text{RCS1}}$.

Note 2: For Flash writes, add the write recovery time, ROMNAL, to the given wait states for ROM high-impedance time.

7.4, 7–19

In the bulleted list beneath the sentence “As a target, the MPC107 responds to a transaction with a retry due to the following,” the fourth item should read as follows:

A configuration write to a PCI device is underway and PICR2[SERIALIZE_ON_CFG] = 1.

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8.7.2, 8–19 In Table 8–4, replace the description for bit 1 with the following:

Table 8–4. DSR Field Descriptions—Offsets 0x104, 0x204

Bits	Name	Reset Value	R/W	Description
—	—	—	—	—
1	EOSI	0	R/W Write1 clears	End-of-segment interrupt 0 No end-of-segment condition. When this bit is set, it can only be cleared by writing a 1 to it or by a hard reset. 1 After the block of data has finished transferring, this bit is set. If CDAR[EOSIE] = 1, an interrupt is generated. Otherwise, no interrupt is generated.

12.1.2.1, 12-4 Replace the third paragraph of section 12–4 with the following paragraph. The only change occurs in the fourth sentence.

When the processor requests data from PCI space, the data received from PCI is stored in the PRPRB until all requested data has been latched. The CCU does not terminate the address tenure of the internal transaction until all requested data is latched in the PRPRB. If the PCI target disconnects in the middle of the data transfer and an alternate PCI master acquires the bus and initiates a local memory access, the CCU retries the ongoing transaction with the processor so that the incoming PCI transaction can be snooped. A PCI-initiated access to local memory may require a snoop transaction on the 60x bus and also a copyback. The CCU does not provide the data to the 60x bus (for the processor to PCI read transaction) until all outstanding snoops for PCI writes to local memory have completed.

13.3, 13–6 Replace the last sentence in the first paragraph of section 13.3 with the following. Note the different ErrDR2 bits.

(The error detection bits are specifically bits 15, 13, and 12 in the PCI status register, bits 7–4 and 2–0 in ErrDR1, bits 6, 3, 2, and 0 in ErrDR2, and bits 8, 7, and 4 in the IMISR.)

B.1, B–1 Replace the final paragraph of section B–1 with the following:

In addition, the PCI bus uses a bit format where the most-significant bit (msb) for data is AD31, while the 60x data bus use a bit format where the msb is DH0. Thus, PCI data bit AD31 equates to the processor's data bits DH0 and DL0, while PCI data bit AD0 equates to the processor's data bits DH31 and DL31.

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B.3, B–3	Replace the final paragraph on page B–3 with the following: Note that the MSB on the 60x bus, D0, is placed on byte lane 0 (AD[7–0]) on the PCI bus. This occurs so D0 appears at address 0x*nnnn_nn*00 and not at address 0x*nnnn_nn*03 in the PCI space.

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